An Approach to Distributed Amplifier Based on a Design-Oriented FET Model

Claudio Paoloni and Stefano D'Agostino

Abstract—**A Design-Oriented FET model in conjunction with an appropriate design procedure for distributed amplifiers is presented. The advantage of including the effects caused by FET parasitics in a newly defined simple unilateral FET circuit to be utilized in the conventional distributed amplifier design procedure allows an accurate prediction of the low-frequency gain and the 3-dB cutoff frequency. The simplicity of this formulation and a set of generalized design charts provide an interesting opportunity to designers. Comparisons among different experimental data from literature and the results obtained by this theory confirm the validity of the Design-Oriented FET model and the effectiveness of the given graphical design method.**

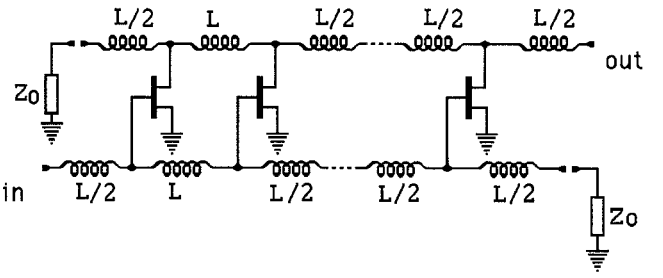

Fig. 1. Schematic of the distributed amplifier.

I. Introduction

THE MULTIOCTAVE behavior of the distributed amplifier makes it one of the most investigated broadband circuits. The apparently simple topology of these amplifiers is actually transformed into extreme analytical complexity for an accurate analysis when FET "parasitics" are included. Most of the design approaches are consequently based on an approximate circuit structure where the FET's are typically included with their unilateral simplified equivalent circuit.

Extensive analyses are presented by Ayliasi *et al.* [1] and Niclas *et al.* [2] showing the limits of an approximate no-loss model with respect to the complete FET model. A first and effective design method is proposed by Beyer *et al.* [3]. It takes into account the losses due to the gate-source and drain-source resistance of the FET included in a unilateral FET circuit. An analytical formulation and a set of design charts are given by the authors to predict the amplifier performance. Further refinements of this procedure were proposed later [4]–[7]. The effectiveness of these design methods lies in their simplicity of use, even though a sensible discrepancy from the real behavior has to be expected. In fact, only the intrinsic FET circuit is considered and the gate-drain capacitance is neglected. Unfortunately, a nonnegligible influence on the overall amplifier performance also results from the extrinsic FET circuit elements.

In this paper, a unilateral Design-Oriented FET model is introduced. The effects of the various elements of the complete FET model are identified and properly taken into account in the recalculated elements of the new simplified FET circuit proposed. In particular, the importance of the effects due to the "feedback" elements in the complete FET model will be shown. The correct formulation of this new simplified model combined with the analytical distributed amplifier design approach from Beyer *et al.* [3] results in an accurate prediction of the performance of the required amplifier. Comparisons with different experimental data from literature are also presented to confirm the validity of the Design-Oriented FET model. Furthermore, an appropriate generalized process independent design technique is also proposed. The validity of this procedure is proven by its application to a published experimental example.

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II. Design-Oriented FET Model

The topology of the distributed amplifier (Fig. 1) is based on a series of FET's properly interconnected by inductances to form an input and output discrete element transmission line together with the shunt parasitic FET capacitances. The FET transconductances electrically couple the two transmission lines. On the one hand, a closer look at the complete FET circuit (Fig. 2(a)) with respect to the conventional simplified unilateral one (Fig. 2(b)), where it is assumed $R_{\mathrm{dse}} = R_{\mathrm{ds}}$, $R_{\mathrm{ie}} = R_{\mathrm{i}}$, $C_{\mathrm{gse}} = C_{\mathrm{gs}}$ and $C_{\mathrm{dse}} = C_{\mathrm{ds}}$)—typically used in the basic theory—makes the level of this approximation clear. On the other hand, any attempt to increase the complexity of the simple distributed amplifier "transmission line" model lead to a dramatic increase in analytical complexity. As a consequence, in all the direct analysis and synthesis methods proposed in literature [3]–[5], the accuracy limit appears to be due to the above mentioned approximate structure. Usually, these procedures provide typical parameters such as low frequency gain and cutoff frequency as a function of the unilateral FET model characteristics. When the performance obtained is compared to the performance of the final realization, a significant discrepancy appears, caused by the oversimplification of the problem.

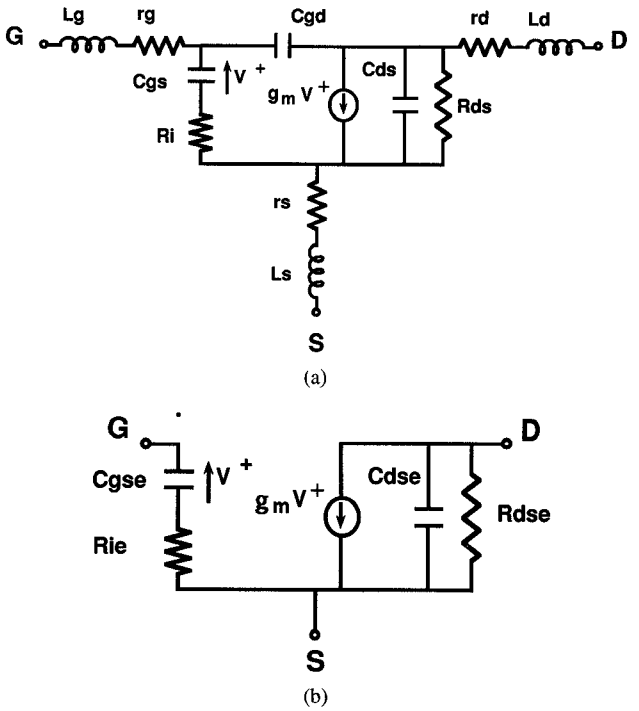

Fig. 2. (a) Complete small signal FET model. (b) Simplified unilateral FET model.

To introduce a higher level of accuracy in the design of distributed amplifiers, a series of considerations follows. The purpose is to obtain a FET model as shown in Fig. 2(b) with recalculated lumped elements, providing a more accurate gain and frequency behavior when utilized in the distributed amplifier's design procedure. The effect of the "feedback" elements such as the source parasitic resistance r_s and the gate-drain capacitance $C_{\rm gd}$ on the low frequency gain A_0 and the 3-dB cutoff frequency $f_{3\,\rm dB}$ was carefully investigated. The FET parasitic inductances typically cause a reduction of the cutoff frequency. However, in the following analyses, these elements will be neglected. This simplifying hypothesis is justified because these inductances are offset by the optimization of gate and drain distributed amplifier "transmission lines" in the final design step.

The analytical approach from Beyer *et al.* [3] proposes a formulation of the distributed amplifier low frequency gain based on the image parameter theory by adopting a simplified unilateral lossy model for the FET. The expression is:

$$A_0 = g_m Z_0 \frac{\sinh(b) e^{-b}}{2\sinh(b/N)} \tag{1}$$

where:

- g_m is the transconductance of the FET;
- N is the number of FET's in the amplifier;
- b is a lossy factor associated with the drain line expressed as [3]:

$$b = \frac{N}{4}\left(\frac{Z_0}{R_{\rm ds}}\right) \tag{2}$$

- Z_0 is the load impedance.

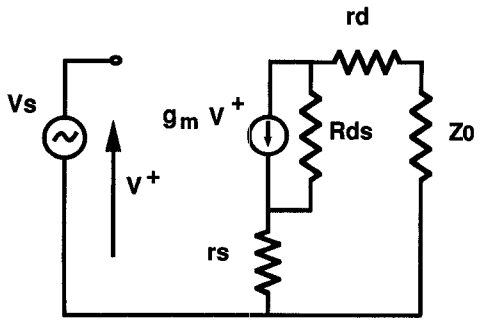

Fig. 3. "Zero frequency" complete small signal FET model.

As a first remark, the low frequency gain is strongly dependent on the transconductance g_m as well as the drain-source resistance $R_{\rm ds}$ of the FET. In fact, as also stated in [3], at low frequency the input line attenuation is negligible, while the output line presents a significant attenuation that is maintained practically constant up to the cutoff frequency.

To take into account the effects of the FET's equivalent circuit elements that can influence the distributed amplifier low frequency gain, an equivalent $R_{\rm ds}$ value ($R_{\rm dse}$) will be now derived. The low frequency voltage gain of the FET is calculated by connecting a voltage generator at the gate terminal and a load ($Z_0 = 50\,\Omega$) at the drain terminal. The "zero frequency" complete model of the FET appears as shown in Fig. 3, since all the capacitances are "open."

After simplifications the voltage gain is:

$$A_v = \frac{V_0}{V_s} = \frac{g_m R_{\rm ds} Z_0}{r_a + R_{\rm ds} + Z_0} \tag{3}$$

where $r_a = r_d + (1 + g_m R_{\rm ds}) r_s$.

The voltage gain for the simplified lossy FET model in Fig. 2(b) is given by:

$$A_{\rm ve} = \frac{V_0}{V_s} = \frac{g_m R_{\rm dse} Z_0}{R^x_{\rm dse} + Z_0} \tag{4}$$

Imposing:

$$A_v = A_{\rm ve} \tag{5}$$

the result is:

$$R_{\rm dse} = \frac{R_{\rm ds} Z_0}{r_a + Z_0} \tag{6}$$

It immediately appears that the $R_{\rm dse}$ value is lower than $R_{\rm ds}$. This makes evident the different behavior of the FET considered with its complete model and with its conventional unilateral model. As a consequence, in the first case there are higher losses on the output transmission line. The role of the feedback source resistance r_s increased by the factor $(g_m R_{\rm ds} + 1)$ in (3) is also evident.

Consequently, when used in the unilateral simplified FET equivalent circuit, the simply calculated $R_{\rm dse}$ resistor imposes a low frequency gain comparable to the gain of the complete FET circuit.

The S-parameter frequency behavior resulting from the complete FET model is due both to the gate losses and the gate-drain feedback capacitor $C_{\rm gd}$. To maintain the unilateral

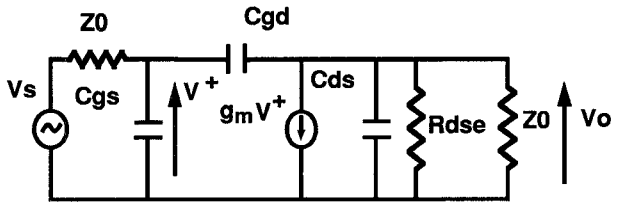

Fig. 4. FET model where the Miller theorem is applied.

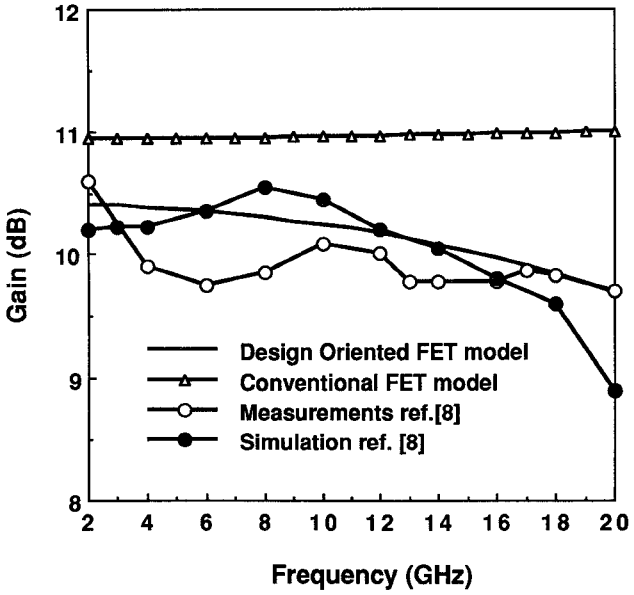

Fig. 5. Comparison between the measured and simulated data reported in [8] and this approach.

approximation, the Miller theorem can be applied to the circuit configuration in Fig. 4 where $R_{\rm ds}$ is substituted by $R_{\rm dse}$ to eliminate the source resistor r_s without losing its low frequency effect. The resistor R_i has also been neglected since its typical low value in this case do not sensibly affect the computation.

Therefore, the new FET capacitance values are:

$$C_{\rm gse} = C_{\rm gs} + C_{\rm gd}(1 - g_a) \tag{7}$$

$$C_{\rm dse} = C_{\rm ds} + C_{\rm gd}(g_a - 1)/g_a \tag{8}$$

where:

$$g_a = -g_m \frac{R_{\rm dse} Z_0}{R_{\rm dse} + Z_0} \tag{9}$$

Finally, we can assume:

$$R_{ie} = r_g + R_i + r_s \tag{10}$$

to include all the lossy effects in the gate mesh of the FET model.

The recalculated unilateral FET circuit including the effect of parasitic resistors r_s, r_g and r_d and the feedback capacitor $C_{\rm gd}$ is thereby obtained. The simplicity of the lumped element expressions lends itself to fast applicability.

The effectiveness of the use of the Design-Oriented FET model in the distributed amplifier design procedure will be now demonstrated by comparison between the prediction obtained by this theory and different experimental data from

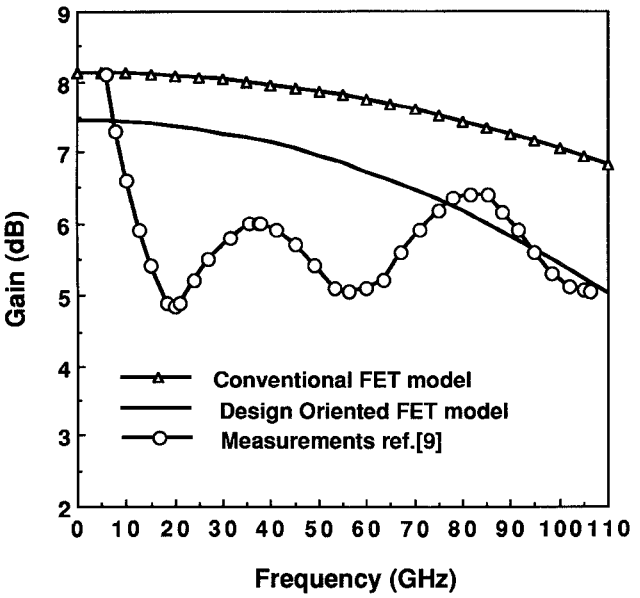

Fig. 6. Comparison between the measured data reported in [9] and this approach.

literature. For each of the published distributed amplifiers considered, the Design-Oriented FET model elements are calculated on the basis of the original FET data and their values are then implemented in (14) in [3] to have the frequency response of each amplifier. These curves are then compared with experimental data of the corresponding amplifiers. To have a complete reference framework, a theoretical simulation with the conventional unilateral FET circuit is also performed.

A five-AlGaAs HEMT distributed amplifier reported by Dixit *et al.* [8] is investigated. The measured and simulated data from literature and the results obtained from the iteration of (14) in [3] using the Design-Oriented FET circuit and the conventional unilateral one are presented in Fig. 5. As a second example, the extremely wide band distributed amplifier consisting of seven InP HEMT's presented by R. Majidi-Ahy *et al.* [9] is also considered, since it is a state-of-the-art application. Measured data provided by the authors in the 5–110 GHz frequency band were compared with theoretical results (Fig. 6) as in the previous case. In both cases, an average FET gate width is adopted since the two amplifiers are consisting of FET's with unequal gate width. Good agreement obtained with respect to the experimental data is evident. It is also worth noting the sensible discrepancy, due to the application of the conventional simplified FET model in both 3-dB cutoff frequency and low frequency gain for all the examples quoted.

III. Design Criteria

Because of the Design-Oriented FET model introduction an appropriate, device technology-independent design procedure is also proposed. The purpose of the method, once the gate width of the chosen FET and the number of FET's composing the amplifier are defined, is to compute the 3-dB cutoff frequency $f_{3\,\rm dB}$ and the low frequency gain A_0 in a reliable manner as a function of the Design-Oriented FET circuit elements.

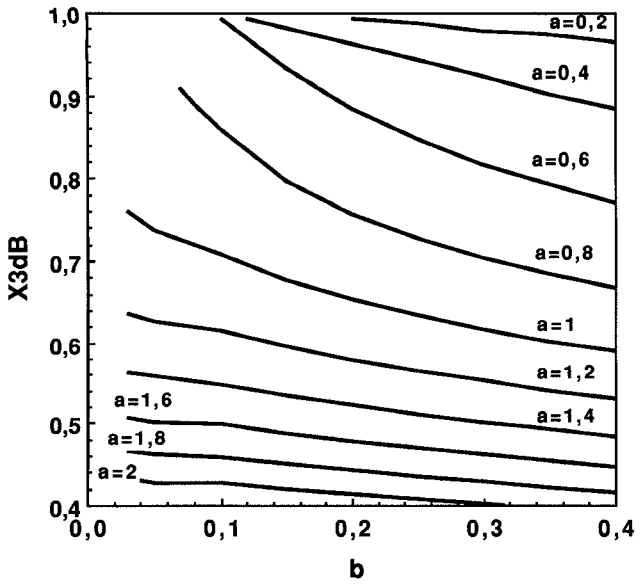

Fig. 7. Chart I: fractional frequency $X_{3\,\mathrm{dB}}$ behavior as a function of the b term.

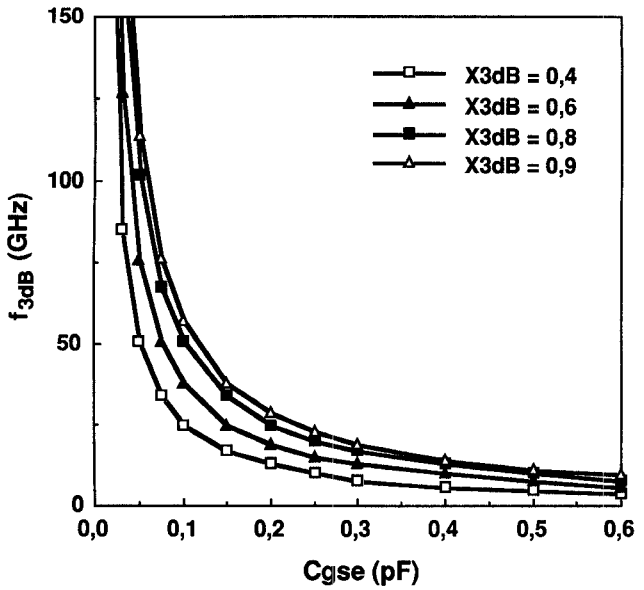

Fig. 8. Chart II: 3-dB cutoff frequency $f_{3\,\mathrm{dB}}$ versus the FET gate-source capacitance C_{gse} for different fractional frequency $X_{3\,\mathrm{dB}}$ values.

The fractional bandwidth term defined in [4] is given by:

$$X_{3\,\mathrm{dB}} = \frac{f_{3\,\mathrm{dB}}}{f_c} \tag{11}$$

where $f_{3\,\mathrm{dB}}$ is the 3 dB cutoff frequency of the amplifier and f_c is the cutoff frequency of the associated artificial transmission line expressed as:

$$f_c = \frac{1}{\pi\sqrt{LC_{\mathrm{gse}}}} \tag{12}$$

where L is the series inductance value according to: $Z_0 = \sqrt{\frac{L}{C_{\mathrm{gse}}}}$. Consequently the 3 dB cutoff frequency $f_{3\,\mathrm{dB}}$ is:

$$f_{3\,\mathrm{dB}} = \frac{X_{3\,\mathrm{dB}}}{\pi C_{\mathrm{gse}} Z_0} \tag{13}$$

Assuming $b \leq 0.4$ [3] the low frequency gain can be expressed in simplified form as:

$$A_0 = 4\sqrt{ab}e^{-b}\frac{f_{\max}}{f_c} \tag{14}$$

where from [3]:

$$a = N\frac{R_{\mathrm{ie}}}{Z_0} \tag{15}$$

and $f_{\max}$ is the FET maximum oscillation frequency [3]:

$$f_{\max} = \frac{g_m}{4\pi C_{\mathrm{gse}}}\sqrt{\frac{R_{\mathrm{dse}}}{R_{ie}}}. \tag{16}$$

After simple algebra the low frequency gain A_0 is given by:

$$A_0 \approx \frac{N}{2} Z_0 g_m e^{-b} \tag{17}$$

The proposed formulation of the 3-dB cutoff frequency $f_{3\,\mathrm{dB}}$ and the low frequency gain A_0 for distributed amplifiers allows to define three design charts to solve the design problem in a generalized and graphical manner.

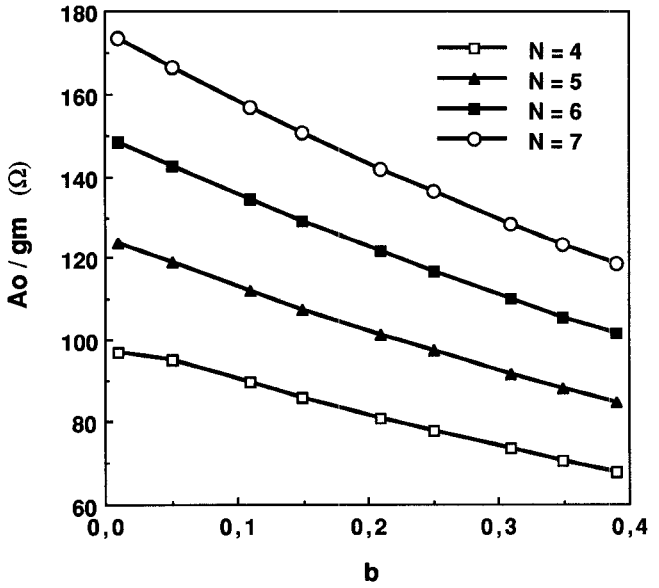

Fig. 9. Chart III: low frequency gain A_0 normalized to the FET transconductance g_m (g_m is expressed in Siemens) plotted as a function of the b factor.

Chart I (Fig. 7) reports the fractional frequency $X_{3\,\mathrm{dB}}$ behavior as a function of the b term for a wide range of a terms. The fractional frequency $X_{3\,\mathrm{dB}}$ is derived from the direct computation of (14) in [3].

Chart II (Fig. 8) plots the 3-dB cutoff frequency $f_{3\,\mathrm{dB}}$ versus the FET gate-source capacitance C_{gse} for different fractional frequency $X_{3\,\mathrm{dB}}$ values. It is worth noting that in both Charts the dependence from the number of FET's composing the amplifier is not relevant under the hypothesis that $N \geq 4$ [3].

The low frequency gain A_0 normalized to the FET transconductance g_m is plotted in Chart III (Fig. 9) as a function of the b factor (the cases for $N = 4$, 5, 6, and 7 were considered). All the plotted values (C_{gse}, $f_{3\,\mathrm{dB}}$ ...) are considered in their typically used range.

TABLE I
COMPARISON BETWEEN THE FET MODELS

FET gate width W=200μm	Design Oriented FET model	Conventional Simplified FET model
R_{dse} (Ω)	384	430
R_{ie} (Ω)	3.54	1
C_{gse} (pF)	0.212	0.15
a	0.354	0.1
b	0.1626	0.1453
A_0/g_m (Ω)	106	108
A_0 (dB)	6.1	6.25
f_{3dB} (GHz)	29.34	38.21
X_{3dB}	0.977	0.9974

Finally, the design procedure can be simply outlined.

Once the number of FET's N and their gate width for the required amplifier is established, the corresponding elements of the Design-Oriented FET model ($R_{\rm dse}$, R_{ie} and $C_{\rm gse}$) and the a and b terms are derived according to (6), (10), (7), (15), and (2) respectively. In (2), $R_{\rm ds}$ is assumed as equal to $R_{\rm dse}$.

The fractional frequency $X_{3\,\rm dB}$ related to the correspondent a and b terms is then obtained from Chart I. The 3-dB cutoff frequency $f_{3\,\rm dB}$ for the given $X_{3\,\rm dB}$ and $C_{\rm gse}$ is taken from Chart II. Finally the normalized low frequency gain A_0/g_m for the required number of FET's N as a function of the b parameter is obtained from Chart III.

It is evident that the generalized nature of this simple procedure enables a fast and reliable evaluation of the design goals of a distributed amplifier.

IV. A Design Application

As example of application of the proposed method the distributed amplifier realization from Niclas *et al.* [10] is adopted. In this particular case, the $C_{\rm dc}$ capacitance appears in the complete FET model, and for computational purposes it is assumed as being equally shared between the $C_{\rm gs}$ and the $C_{\rm gd}$ capacitances. This simplifying assumption has been found not to affect significantly the validity of the procedure.

Also in this case, given the number of FET's ($N = 5$) and their gate width (200 μm), first the Design-Oriented FET circuit elements are calculated and then the proposed design method is applied. Table I lists the obtained FET parameters and distributed amplifier characteristics. It is evident how significantly the FET-lumped element values in the Design-Oriented FET model case differ from those in the conventional simplified FET model. As a direct consequence, the low frequency gain A_0 and, more dramatically, the 3-dB cutoff frequency $f_{3\,\rm dB}$ are modified by the application of this theory, allowing for a more accurate performance prediction.

The comparison between the experimental results from [10] and the computed curves by (14) in [3], using both the Design-Oriented and the conventional simplified FET models is presented in Fig. 10.

Furthermore, for a given technological MMIC process the three charts can be effectively summarized in a single chart

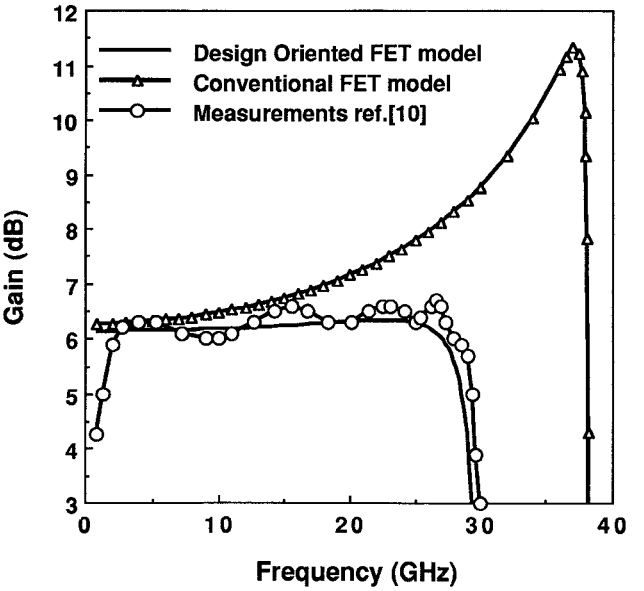

Fig. 10. Comparison between the experimental results reported in [10] and this approach.

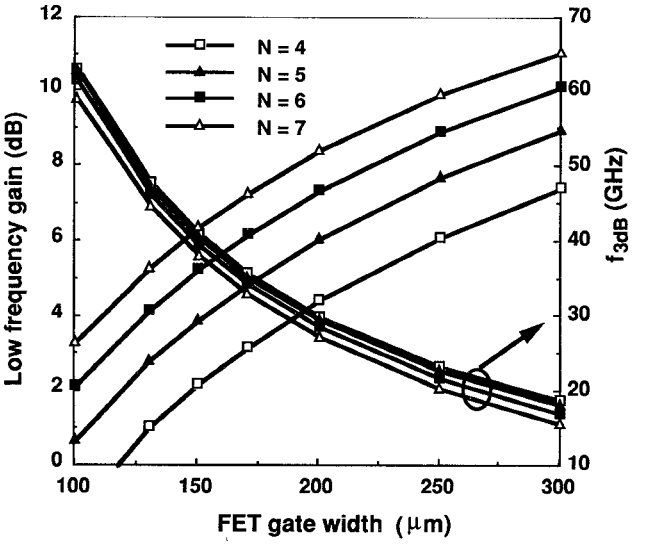

Fig. 11. An example of distributed amplifier Synthesis Chart for a 0.25-μm HEMT gate length MMIC process [10].

suitable for a direct distributed amplifier synthesis (Fig. 11). As an example, the above mentioned process by Niclas *et al.* [10] is considered again and the typical MMIC FET parameter scaling features are also applied. The Synthesis Chart presented enables a direct evaluation of the required FET gate width and the correspondent low frequency gain A_0 for a distributed amplifier with a specified 3-dB cutoff frequency $f_{3\,\rm dB}$ and a N number of FET's.

V. Conclusion

A new simplified lossy unilateral FET model oriented to the design of distributed amplifiers has been proposed. The simplicity of this circuit allows for fast applicability and accurateness. In conjunction with conventional design methods, it provides a reliable evaluation of the real performance of the required distributed amplifier with respect to previous approaches.

A graphical design procedure related to the Design-Oriented FET model has also been presented. The design Chart-based method proves to be effective in the direct prediction of the amplifier performance. A Synthesis Chart related to a given technological MMIC process is also presented. The comparison with literature cases brings forth a reliable demonstration of the validity of the proposed FET model.

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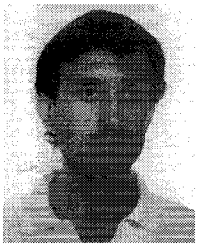

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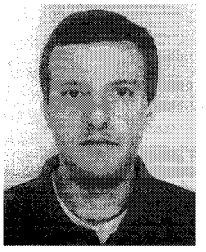

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